# dsp valley newsletter 6

## designing smart products

# AnSem - Tracking marine animals with SATCOMS

Satellite monitoring of wildlife has become a critical tool for environmental research and nature preservation. In acknowledgement of this, ESA has been supporting the development and testing of a new low-cost wildlife tag. Currently being developed in an on-going ARTES 5.1 activity, the new system works in conjunction with the Argos satellite monitoring system, a non-profit initiative established in 1978 that is dedicated to helping the research community monitor

and better understand the environment. Argos is operated by CLS (FR), a leading provider of satellite services for environmental and maritime applications.

The new tag developed in this ARTES 5.1 activity has a tiny transmitter powered by a battery or a solar panel that sends messages of short duration (less than one second) to the Argos constellation, whose six satellites circle at 850 km in polar sun-synchronous orbit, meaning they pass over a given location on Earth at approximately the same time each day.

**continuation from page 1**

Currently available wildlife tags that use the Argos 1/2 first-generation satellite services are rather inefficient, with poor battery life and low data collection volumes. The goal of this ARTES project is to develop a low-cost tag which can take advantage of the newer, more sophisticated Argos 3/4 services. With the support of ESA, a new microchip, called ARTIC, was developed by the Belgian semiconduc-



*Photo: Star Oddi*

*Marine animal tag with silicon coating. Initially the new tag will be used to track migrating marine animals, as this is the biggest challenge from a technology point of view, but in the future it could be used for terrestrial wildlife and birds as well.*

tor company AnSem; it is now being integrated into a new animal tagging system by the Icelandic company Star Oddi.



*Blue shark, South Africa. Photo: ESA/P. de Maagt*

The key improvements include smaller weight and size, increased lifetime, expanded data storage, and bidirectional communication with the satellite, which results in improved data transfer rates.

The latest version of AnSem's ARTIC has 250 mW transmitting power, sufficient to be able to reach the satellite without an external power amplifier. It contains sensors for pressure (depth), temperature, light and tilt, the latter to allow 3D mapping.

*"Bidirectional communications are key here,"* says Stefan Gogaert, CEO of AnSem. *"Without it, the tag keeps continuously uploading data, which takes a lot of power. With the bidirectional communications supported by Argos 3/4 and implemented in this ARTES 5.1 project, we introduce a handshake sequence so that the tag knows that the data have been received by the satellite. This radically improves battery life."*

These first samples of the ARTIC chip have passed certification at CLS. In the next stage of the project, commencing in June 2016, five bluefin tuna and five basking sharks will be tagged to validate the new system. *"In mid-2016, we hope to start commercial production of*
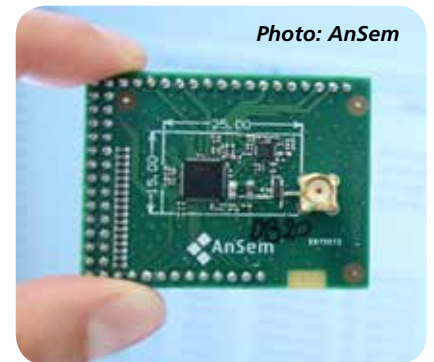


*Photo: AnSem*

*AnSem's ARTIC ASIC for Argos 3/4.*

*the ARTIC chips,"* says Gogaert.

*"There are competing satellite monitoring systems in use, but the advantage of*

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# A New Alliance was born

During 3 years, DSP Valley has been building the foundations for a strong European inter-cluster cooperation in the semiconductor domain. Together with the clusters of Silicon Saxony in Dresden (DE), Minalogic in Grenoble (FR) and High Tech NL in Eindhoven (NL), later also joined by ME2C in Villach (AT) and Business Cluster Semiconductors in Nijmegen (NL), we have been building a strategy on how to strengthen the competitiveness of

our cluster members, including multinational companies as well as local start-ups, spin-offs and SMEs, based on an inter-cluster cooperation model.

This strategy is ready now. We have been developing a Joint Action Plan, completed with an Internationalization Plan and a Financial Plan. According to this Joint Action Plan, we will create value for our members by promoting transnational transfer of knowledge

and technologies between the cluster members, by giving improved visibility on the potential of micro/nano electronics as the key enabling technology for lots of applications in various markets, by encouraging and supporting SMEs to participate in European projects and by giving them access to public and private funding, and last but not least, by exploring and promoting international market opportunities.

*Argos 3/4 is low output power require-ments and small size,"* says Michel Guigue, Data Collection and Missions Manager at CLS. *"We can provide solar satellite tracking solutions as light as 2 or 3 g with output power of just 200 mW. Argos uses a basic satellite com-munication protocol which makes the system very robust in harsh conditions. Other systems require larger modems that need at least 2 W output power and very good conditions, such as you find on land. For birds and fish, Argos is the only option."*

*"The monitoring of migrating marine animals is essential for understand-ing the impact of global changes and increasing human activities on the marine eco-system,"* says Peter de Maagt, Head of the Antenna and Submillimetre Wave Section at ESA. *"This ARTES-supported project should make an important contribu-tion towards that aim, and eventually improve our knowledge of many differ-ent kinds of wildlife."*

*"This activity shows how ARTES can both benefit society and push techno-logical advancement at the same time,"* de Maagt says.

■

**Now we are ready for action!**
Strongly believing in the success of inter-cluster cooperation, and continu-ing on some successes we have already unlocked for the cluster members during the strat-egy preparation phase, we have unanimously decided to continue

# Philips AmbiLux UHD TV debuts Ambilight projection for the ultimate immersive viewing experience – TP Vision

TP Vision launches the new Philips AmbiLux TV that will take the immersive viewing experience to a superb new pinnacle with 4k Ultra HD and introduc-ing Ambilight projection technology, the most significant development yet for the unique Ambilight system. The R&D for this 65inch Philips AmbiLux model, including the Ambilight pro-jection technology, was done by TP Vision's Innovation Site Europe in Ghent and will reach the shelves during the fourth quarter.

The classic Philips Ambilight system uses rows of LEDs mounted on the rear of the set to create a colored halo of light on the wall behind the TV. The colors precisely match the on-screen content to create the impression of a larger image and to provide a more enjoy-able viewing experience. The revolu-tionary Ambilight projection technology now frees the actual images from the constraints of the set by using nine tiny pico-projectors, each precisely posi-tioned on the rear of the AmbiLux TV. Intelligent overlap technology allows a seamless projection of the onscreen image, motion and color on to the rear wall surrounding the set. Precision tech-nology ensures that the Ambilight pro-jection system can project images with superior clarity, vivid color and supreme contrast to create an immersive experi-ence that truly breaks the boundaries of TV viewing.

Further developments in Ambilight tech-nology take the system beyond just films and TV and can enhance the enjoyment of music too. The new Ambilight Music Mode provides a colored halo of light that can follow and react to the dynam-ics of any music played through the TV,

whether via a streaming service such as Spotify, USB or a music channel. Consumers can choose from a variety of colorful pre-sets or simply select the ran-domizing party mode. Integration with the popular Philips Hue Smart Lighting takes Ambilight even further by provid-ing a whole room experience for total 360° immersion.

Despite adding the rear-mounted pro-jectors and powerful processing, the AmbiLux has been beautifully engi-neered to maintain a razor-slim, elegant form. European design and authentic, premium materials ensure a high qual-

ity finish with the ultra-narrow bezel, achieving a seamless connection to the Ambilight halo, and the polished chrome Bladewire stand creating a light, floating appearance. The sophisticated design allows the AmbiLux to effort-lessly enhance even the most stylish of interiors.

■

# DAB-Embedded brings new platform for medical applications.



DAB-Embedded company presents its new product : DAB-MED-AM5 system-on-module, which is based on the new AM5728 processor from TI.

This is dualcore ARM Cortex-A15 @ 1.5GHz with a rich peripheral set like video input ports, 3x LCD & HDMI outputs, additional Dual DSP C66x with IVA HD Video coprocessor. This SoC has enhanced the graphical subsystem: 3D accelerator – dualcore SGX544, 2D accelerator – GC320.

Additionally the SoC has IPU (Image Processing Unit) blocks based on ARM Cortex-M4 cores and a specialized ICSS unit for real-time control and industrial communication.

A number of well-known interfaces like SPI/UART/I2C/CAN, USB 2.0/USB 3.0, Gigabit Ethernet, SATA and PCIe gives you access to external devices or your sensors.

We combine all required components on a single PCB, for instance:
- AM5728 processor:
  - 2x Cortex-A15 CPU cores @ 1.5GHz;
  - 2x C66x DSP cores @ 700MHz;
  - 2x Imagination Power VR SGX544 3D GPU cores @ 533MHz;
  - Vivante GC3230 2D BTBLT accelerator;
  - 2x Cortex-M4 microcontroller cores @ 167MHz;
  - PRU-ICSS programmable subsystems (4x cores)
- Memory:
  - DDR3 with ECC (up to 2GB);
  - 4GB to 32GB eMMC flash;
  - Up to 16MB QSPI NOR flash;
- Networking — 2x gigabit Ethernet controllers (1x PHY);
- Power management system (based on TPS659037);
- Onboard 1Gbit Ethernet PHY;
- WiFi + Bluetooth module (2.4GHz/5GHz dualband WiFi, Bluetooth 4.1 + BLE);
- All necessary clock generators (including SATA and PCIe);

- SAMTEC connectors with all necessary signals (all GPIOs and peripheral I/Os) from AM5728:
  - HDMI output (up to 1920 x 1080);
  - Parallel RGB (24-bit) at up to 1920 x 1200;
  - 8x audio (including 6x I2S);
  - 3x CPI camera;
  - USB 3.0 host/client;
  - USB 2.0 host/client;
  - SATA 2.0;
  - 2x CAN;
  - 2x MMC/SD/SDIO;
  - 4x SPI/SSP;
  - 5x I2C;
  - 8x UART;
  - 2x PCIe Gen 2;
  - GPIO, PWM, JTAG, keyboard, McASP.
- Power supply +5V.

The system-on-module provides software support based on Linux 4.1.6, Windows Embedded Compact 2013, in the future - Windows 10 IoT.
DAB-Embedded additionally provides:
- software packages (for example projects for building DSP applications (C66x-based, GCC-examples, CCS-examples), ARM Cortex-A15 applications, PRU-ICSS examples, and Cortex-M4 examples);
- software support for fast hardware and software integration;

# Macnica Americas and intoPIX bring a new FPGA reference design for UHD4K Live production over IP, using RTP transport and TICO lite compression

## The new design running on an Altera FPGA achieves low latency, visually lossless UHD4K transport over 10GbEthernet network infrastructures



Macnica Americas, a leading supplier of video over IP solutions, and intoPIX, a leading provider of compression technologies, have demonstrated a new FPGA solution designed to carry UHD4K

over IP in studio infrastructure, using TICO lightweight compression over RTP at the SMPTE 2015 Annual Technical Conference and Exhibition, Hollywood, California. The demonstration featured

an Altera FPGA development kit using an Altera HDMI 2.0 IP core with UHD 4K 60 frames per second input in 4:2:2, intoPIX TICO IP cores doing the encoding, and Macnica Americas IP cores doing

### About Macnica Americas

Macnica Americas is a design services and IP provider with expertise in video transport solutions. Macnica's IP portfolio includes solutions for Broadcast Video and Pro AV (specifically SMPTE 2022-1/2/5/6/7 IP) as well as high speed networking and embedded applications.

**AM572x**

our cooperation for the deployment of the action plan! Even more, we have decided to widen the inter-cluster cooperation to additional cluster partners: NMI from the UK, MIDAS from Ireland, SCS from France, GAIA from Spain, Mi-cluster from Greece and Distretto Green and High Tech Monza Brianza from Italy.

This is our new Silicon Europe Alliance: an inter-cluster cooperation alliance with the 12 leading European semiconductor and micro/nano electronics clusters, now ready for deploying a strong action plan for strengthening the competitiveness of our cluster members.
I am looking forward to creating a lot of successes at the benefit of our European semiconductor industry! Looking forward to helping also your organization in strengthening your competitiveness!

Best regards,
Peter Simkens

Managing Director
DSP Valley
Chairman Silicon
Europe Alliance
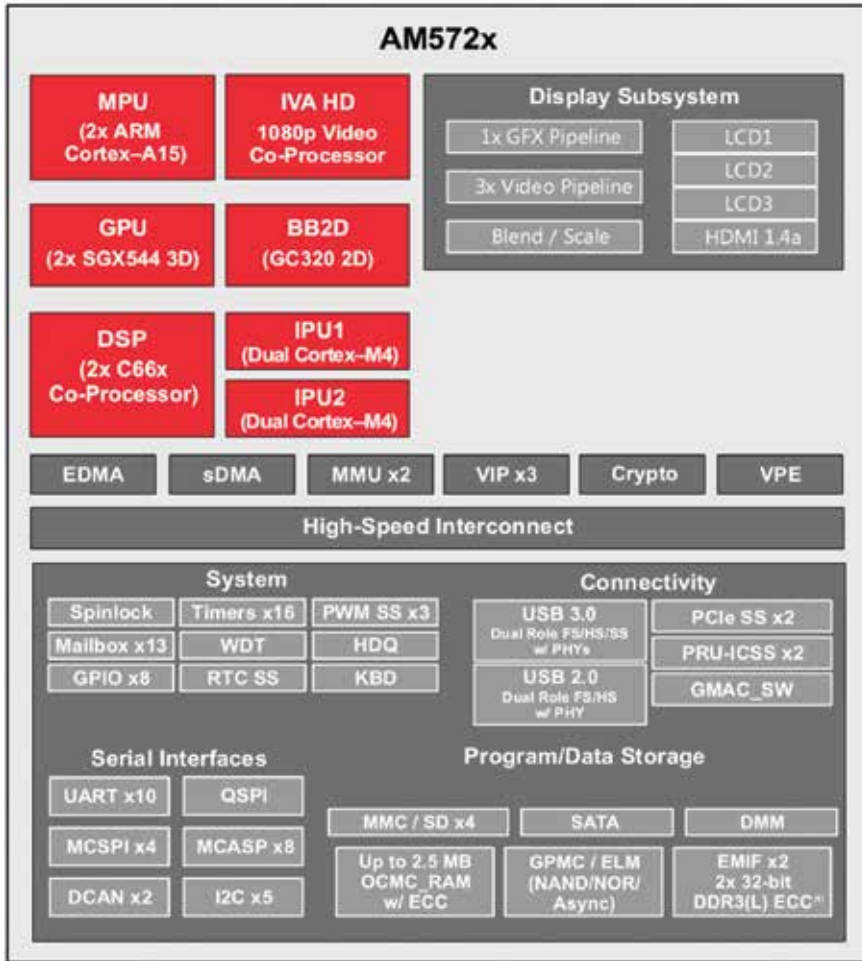
- trainings for software integration for DSP C66x, ARM Cortex-A15 cores and AMP integration;
- base board design services.

Besides, DAB-Embedded can provide video processing libraries (based on correlation filters or neural network) for noise reduction on images, complex object recognition in video stream and more. ∎

the mapping over RTP and transport over 10GbE. A very low latency can be achieved with a minimum of 9 pixel lines in total and a compression up to 4:1.

*"Altera's close collaboration with our partners, intoPIX and Macnica, enables our customers to transport true 4K60 video over 10GbE as well as show the seamless translation to Altera's HDMI 2.0 IP. This is another significant step in making IP networks in a video workflow a reality,"* said Umar Mughal, Altera, Director Broadcast Business Unit.

*"IntoPIX's TICO Codec is the perfect fit for RTP transport solutions. The video quality is truly visually lossless, and occu-*

*pies the same bandwidth as a 1080p stream. We value our partnership with IntoPIX to bring flexible IP transport solutions to Broadcast customers,"* said Marc Levy, Macnica Americas, CTO.

*"Macnica Americas is the first provider of a full reference design solution based on TICO lightweight compression with RTP mapping to carry UHD-4K over 10GbE IP suitable for new IP-based studio infrastructures. intoPIX and Macnica Americas have already successfully worked together to bring a VSF TR01 JPEG2000 over TS and ST2022-1/2 design. With this new reference design, we are together again accelerating the market migration towards IP-based*

*ecosystem,"* said Gael Rouvroy, intoPIX C.T.O.
∎

### About intoPIX

intoPIX is a leading image compression technology provider to audiovisual equipment manufacturers. We are passionate about offering people a higher quality image experience and have developed FPGA and ASIC IP-cores as well as software tools that enable leading-edge TICO Lightweight compression, JPEG 2000 compression, security, video over IP and hardware enforcement.

**Preface**

# Caeleste: Supplier of beyond state of the Art Custom CMOS Image sensors

Caeleste was created in December 2006, by a few people around the former CTO of Fillfactory/Cypress. After an organic growth start, Caeleste is now 22 persons large and fast growing with a CAGR of 30-50%. It is specialized in the design and supply of custom specific CMOS Image Sensors (CIS). Caeleste is still 100% owned by its founders.

Although the company is relatively young, the staff members have a track record of over 150 years in image sensor design and characterization in companies as such KU Leuven (ESAT),

IP Portfolio, related to low noise and high dynamic range sensors, to photon counting, to X-ray pixel design, to time gating pixels, TDI and finally to proton and Single Event hardened pixels.

Since 2015 Caeleste is also a member of DSP Valley in the Smart imaging group and a follower of the Smart health activities.

Caeleste is still a pure play custom design house. We do not have a standard product portfolio and we do not have to prioritize internal developments with respect to customer needs. In fact Caeleste has almost the largest CIS design team in Europe, exclusively devoted to customer specific CMOS

guarantee a flawless delivery of packaged and tested imagers in production.

Besides the realization of custom specific projects, we run also internal R&D projects to test new image sensor concepts in the selected foundries in order to explore further the limits of the imaging technology. These R&D projects resulted in Beyond State of the Art Image Sensors with low noise and very high dynamic range; some highlights are explained more in detail:

- Caeleste has the world record in low noise imaging: We have proven a noise limit of 0.34 e-rms; this implies that under low flux conditions (e.g. in astronomy) each and every photon can be counted and that the background is completely black, provided that the dark current is low enough.
- Caeleste has also designed a dual color X-ray imager, which allows a much better discrimination and diagnosis of cancerous tissue than the conventional grey scale images (see figure).
- Caeleste has also its own patents for 3D imaging, based on Time of Flight (ToF) operation. This structure allows the almost noise free accumulation of multiple laser pulses to enable accurate distance measurements at long distance or with weak laser sources.
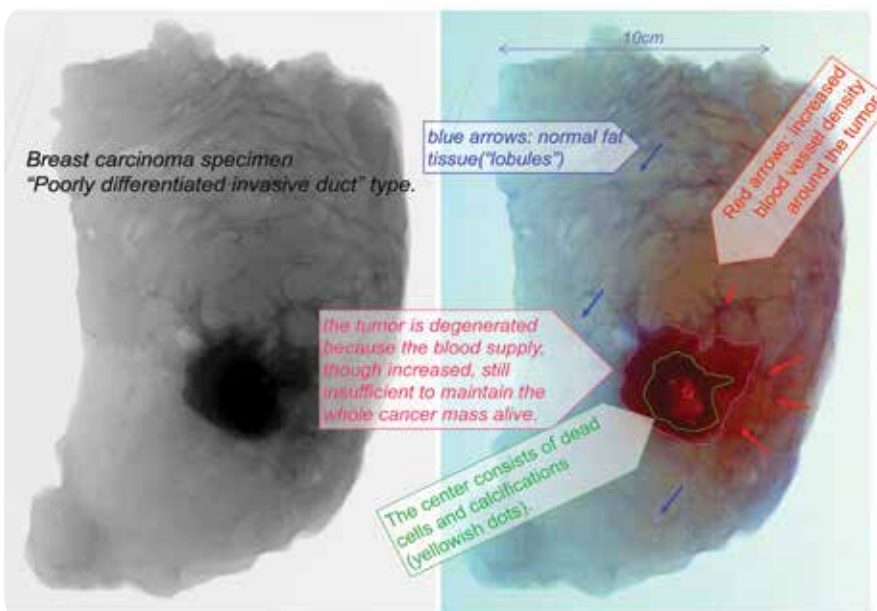


*Breast carcinoma specimen: comparison of a conventional grey scale X-ray image (left) with a dual color image. Resolving the energy allows to discriminate between normal fat and blood rich tissue.*

imec, TU Delft, FillFactory, Cypress Semiconductor, ON Semiconductor, Melexis, Xenics, Canberra. Its sensors are used in medical imaging, industrial vision, scientific cameras and instruments and also in space applications (for remote sensing and science experiments). Caeleste has a patented

image sensors. Caeleste is collaborating with the most renowned, open foundries for CMOS image manufacture and with ultra-clean assembly and test houses. Due to these collaborations, Caeleste can design your image sensor and deliver prototype samples under the best possible conditions, but it can also

## About Caeleste

Caeleste (°2006) is a supplier of custom designed image sensors for the most demanding applications, active in Medical, Space, Automotive, Scientific and Instrumentation imaging, focusing on high-speed imaging, high dynamic range and single photon detection.

# Fuji Xerox Reduces Silicon Area by More than 50 Percent Using Synopsys ASIP Designer

**SYNOPSYS®**
*Silicon to Software™*

## Synopsys' Application-Specific Instruction-Set Processor Tool Enabled Rapid Exploration and Optimization of Processor Architecture for Multi-Function Printer Application

### Highlights:

- Fuji Xerox reduced silicon area by more than 50 percent using an application-specific instruction set processor (ASIP) developed with ASIP Designer, compared to fixed hardware

- ASIP Designer's "compiler-in-the-loop" technology enabled use of application code to optimize the processor architecture for performance, power and area

- Automatic generation of software development kit and synthesizable RTL enabled Fuji Xerox to complete the entire design in less than 14 months

Synopsys, Inc. (Nasdaq:SNPS) has announced Fuji Xerox Co., Ltd. used Synopsys' ASIP Designer tool to design a high-performance application-specific instruction set processor (ASIP) for its full-color multifunction printer. With ASIP Designer, Fuji Xerox developed a specialized instruction-set custom processor that consumed less than 50 percent of the die area of a fixed hardware implementation while still meeting the performance requirements. In addition, unlike fixed hardware, an ASIP offers software programmability, providing the flexibility Fuji Xerox needed to meet the varied processing demands of its multifunction printer application. Using ASIP Designer, Fuji Xerox's design team was able to complete its ASIP design from concept to implementation in less than14 months.

*"Synopsys' reputation as the premier provider of ASIP development tools was the key factor in our decision to use ASIP Designer for our custom processor development,"* said Noriaki Tsuchiya, manager of the Controller Development Group at Fuji Xerox Co., Ltd. *"ASIP Designer's rapid architectural exploration capability made it possible for us*

*to immediately profile the architecture against our algorithms. Designing an ASIP with an instruction set and functional units tailored to our application domain enabled us to significantly reduce gate count, while achieving our required system performance of printing 70 pages per minute."*

While angularity correction is typically done mechanically, the need for quiet



operation in office automation equipment required Fuji Xerox to take the different approach of using advanced image processing algorithms to apply the correction to the scanned image. To implement this in a performance- and area-efficient way, with the flexibility to make modifications to the algorithm, Fuji Xerox chose to design a custom processor using Synopsys' ASIP Designer tool.

Synopsys' ASIP Designer allowed Fuji Xerox to use a high-level specification of the processor to quickly model multiple processor architectures. Using this single input specification, ASIP Designer automatically configured the software

development kit (SDK) containing an instruction-set simulator (ISS), assembler, linker, debugger and C compiler, and also generated the synthesizable RTL design. The immediate availability of the C compiler and the ISS, including its advanced profiling capabilities, enabled the unique "compiler-in-the-loop" methodology, allowing Fuji Xerox to rapidly profile the performance and tune the architecture for its specific image pro-

cessing algorithms written in C.

*"By replacing fixed hardware with ASIPs, companies like Fuji Xerox can significantly reduce total system cost, while increasing the overall flexibility of the design,"* said John Koeter, vice president of marketing for IP and prototyping at Synopsys. *"Fuji Xerox's implementation of an ASIP for image correction in their multi-function printer illustrates how Synopsys' ASIP Designer tool enables designers to rapidly explore and optimize processor architectures to achieve the best balance of programmability, performance and area, while accelerating the development of their SoC."*
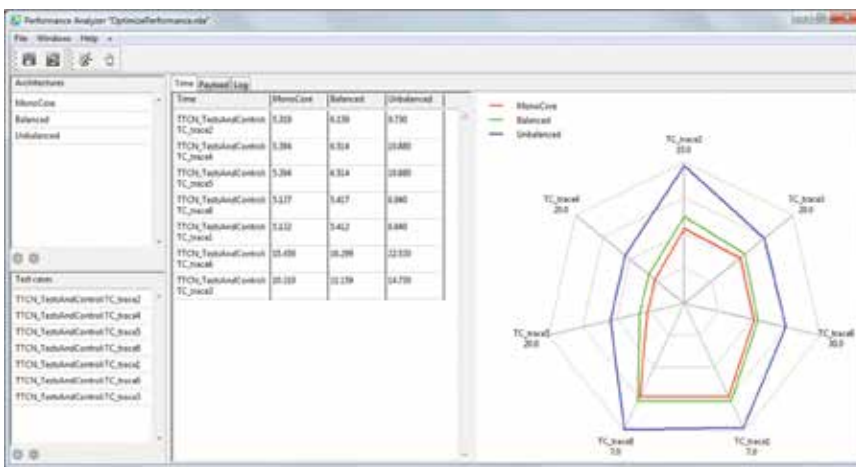
# PragmaDev - Find the best architecture



Following Moore's law, multi-core processors are now more and more common in embedded systems. But to get the best of the parallel processing power it is important to choose the right allocation of resources. If not carefully studied it might happen a multi-core architecture will end up with lower performances than a mono-core while consuming much more energy. For example if the flow of execution does not actually have enough parallelism, the waste of time to synchronize the cores is not balanced by the gain of parallel processing. The same question occurs in any distributed processing system and not only the performance is of interest, but also the energy efficiency.

For that matter three types of information are required:

1. A set of usual functional scenarios. Scenarios that are likely to be executed, on which performance optimization is to be investigated.
2. The possible architectures including their characteristics such as the processing throughput of each available resource.
3. Measures of the time spent to execute an action relatively to the processing throughput available.

The first two types of information are generally quite straight forward, but the estimate or the measurement of the corresponding execution time is definitely trickier to get. Experiments on real targets are usually required to get a proper estimate of performance.

As a technological provider we have always preferred very precise models of execution and in particular executable models. For testing we also use a standardized executable test case notation. So we found out that if we added



*Exploration of the different scenarios for the possible architecture. The results are displayed in a radar graph for easy reading.*

## Antmicro - Emul8: The Open Source Embedded Systems Emulator



DSP Valley Associate Member, Antmicro, a company specializing in embedded systems innovation, new product development and assisting customers in the adoption of new technologies, together with their partner Realtime Embedded are happy to announce the much awaited open source release of Emul8 - an embedded systems emulator that might just become a new favorite tool of the trade for professional developers in the industry.

The official launch took place at Embedded Conference Scandinavia, held in Stockholm over November 3rd-4th, 2015.

With embedded systems becoming more complex and challenging in terms of design, development and deployment, Emul8 comes in as an easy and readily-available solution for iterative development and continuous integration of devices or systems of devices in a fully controlled environment, even if the physical hardware is not yet available.

The tool has been in development since 2010, and by making it open source, a broad audience of developers and companies can be reached and further tools, platforms and functionalities can be added on top of the already richly-featured project. The possibilities today include creating, testing and debugging software based on various operating systems like Linux, FreeBSD, Android, Contiki, RIOT, FreeRTOS or eCos on top of various platforms from vendors like Freescale, Texas Instruments, STMicroelectronics or Nvidia.

### What exactly is Emul8?
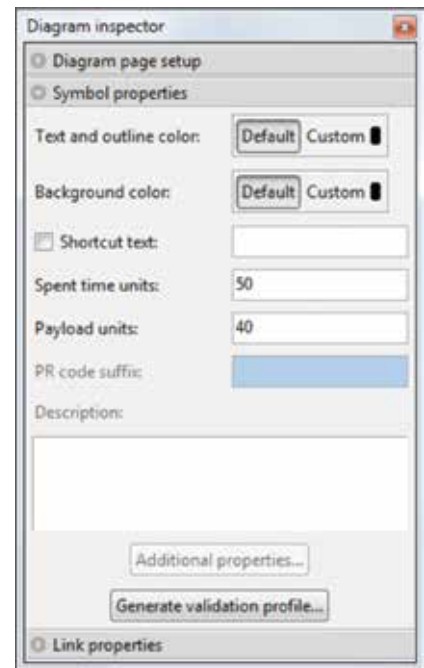Emul8, as the name suggests, is an emulator that targets various embedded
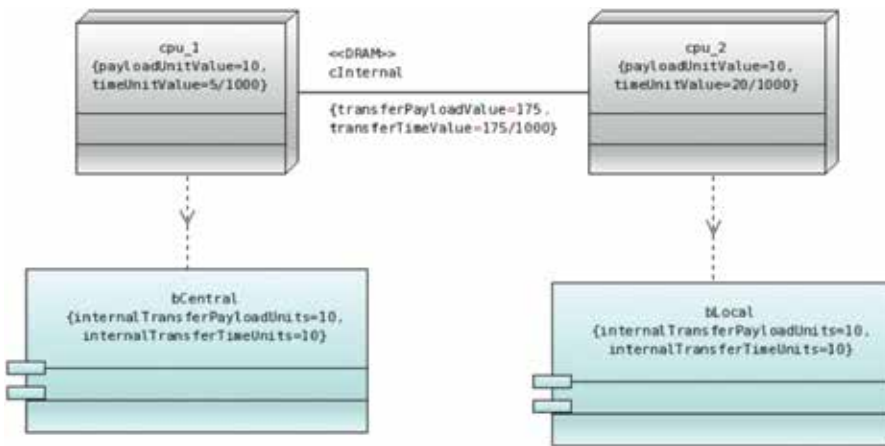
*Definition of a possible architecture.*



*Time spent for execution of an instruction.*

timing information to any instruction in our model, with a number of simulations driven by nominal test cases, we could deduce the performance for each architecture; and therefore find the best one. That is what we have called the Performance Analyzer.

From a technological point of view we use:
- An executable model designed with SDL (Specification and Description Language Z.100 standard from ITU-T), enriched with estimated performance for any atomic instruction.
- A set of functional test cases with TTCN-3 (Testing and Test Control Notation Three Z.160 standard from ITU-T).
- A set of possible allocations described with UML Deployment Diagram (standard from OMG), with the throughput of the respective nodes. ∎

## About PragmaDev

PragmaDev provides a set of modeling and testing tools for the development of real time and embedded software: Real Time Developer Studio. RTDS provides three levels of modeling: informal, semi-formal, and fully formal. While informal modeling, the most common, is mainly used for documentation; the most advanced level of modeling allows simulation, prototyping, verification, full code generation, debug on target, test generation, and test of the model.

systems, typically based on ARM CPUs and/or MCUs (there is also support for SPARC, PowerPC and x86). With Emul8 you can develop your system entirely in a virtual environment that runs within your PC.

Emul8 is an Instruction Set Simulator (ISS), meaning it offers functional simulation of an embedded device or set of devices at the instruction level, and it is built for speed necessary to do iterative software development without getting irritated. Typically, you can work with your code in Emul8 more effectively than you would on real hardware, with comparable execution times but without the overhead of e.g. reprogramming the device or rerunning to produce more debug output.

### How is Emul8 useful?
Running embedded software in a PC abstracts out the physicality of a real embedded system - since you are working in a fully controlled environment, you can monitor and influence all the elements in the system, something that is difficult in typically constrained embedded device, where debug output is scarce and the real state of the system unknown and hard to trace.

Emul8 lets you create repeatable, scriptable, virtual devices or systems of devices that can execute your real code for the purpose of development, testing and debugging. If used in the right scenario, it can greatly improve your and your team's productivity, by letting you create identical and controllable development environments which can

be analyzed and automated much easier than many hardware-based setups.

### How do I get started?
You can simply get in touch with us via our website: http://emul8.org/ or at info@emul8.org ∎

## About Antmicro

Antmicro is an embedded technology company providing SW/FPGA development services for the emerging ecosystem of the Internet of Things. We are enablers of new technologies and skilled integrators, helping customers create smart, innovative products.

# Fully automated human digestion simulator for unprecedented scientific testing – the T&M Solution

## SHIME® — a bio-simulation unit by ProDigest, in partnership with Test & Measurement Solutions

Apart from scrutinizing gastric and intestinal processes, ProDigest also develops lab equipment to artificially fabricate the complete digestive system of humans and animals. The Ghent University spin-off has developed a unique, fully automated bio-simulation unit. To achieve this, the company worked with Test & Measurement Solutions (T&M Solutions) — to be able to provide a fitting monitoring solution.



### Background and challenges

How to measure the effect of food supplements on the bacterial flora of the large intestine? For one, you would need to collect regular in-vivo samples without influencing the digestive process: a daunting task – if not impossible – at least without the proper technology. That's why ProDigest designed SHIME®, choosing T&M Solutions as its partner for the design and installation of its monitoring equipment.

Short for 'Simulator of the Human Intestinal Microbial Ecosystem', the unit lives up to its name:

- **Five glass reactors**, placed on stirrers, simulate the functions of the stomach, the small intestine and three areas of the large intestine;
- For comparative purposes, each unit consists of **two such systems**: one that mimics the digestion of specific

food supplements, and one that represents regular digestion;

- To study both human and animal digestive mechanisms, a variety of simulated body temperatures and digestive products are used;
- Every simulation cycle runs 24/7 over the course of about two months, which means SHIME® needs to be able to operate **automatically**.

### The T&M solution

*"SHIME® digestive systems need to be 'fed' three times a day"*, explains Pieter Van den Abbeele, Senior Scientist at ProDigest. *"Digestive enzymes therefore also have to be added on a regular basis. The contents should move from one reactor to another. Several probes ought to closely measure and monitor pH levels and redox reactions. And, if needed, pumps need to be automatically controlled in order to adjust these chemical features."*

In short: the need for an automated electronic and mechanical solution was beyond dispute. T&M Solutions has developed custom electronics to record and stabilize signals from the pH probes and redox potential measurement equipment:

- A field-programmable gate array (FPGA) processes these signals, communicating about 100 inputs and outputs to a National Instruments sbRIO controller.
- This control device then ensures that the pumps are functioning correctly, taking into account all relevant control curves.
- The SHIME® controller was programmed in a LabVIEW environment from A to Z, making it possible to communicate the measuring signals to the hardware via the NI drivers.
- Embedded in Windows 7.0, the instal-

lation's PC-based interface is intuitive to use and guarantees a very detailed overview of all relevant parameters.

*"We have also included an uninterrupted power supply (UPS) system in the electronics set-up"*, adds Koen Schoofs, Sales Manager at T&M Solutions. *"That way, we avoid weeks of analyses going to waste in the event of a power fail-*



*ure. And to make SHIME® even more reliable, the whole installation is based on fanless solid-state technology, using circuits and devices built entirely from solid materials."*

### Results

With the assistance of T&M Solutions, ProDigest now has seven reliable SHIME® simulators up and running, thereby offering high-quality services to its clients across the globe. This enables the



company to capitalize on the growing need for research on food supplements and their impact on the human digestive mechanism. To refine this research process even further, ProDigest and T&M Solutions are already working on fine-tuning this one-of-a-kind bio-simulator.

# UGent HES group leads European project on run-time reconfigurable computing

The Computer Systems Lab HES team (Hardware and Embedded Systems) of Ghent University coordinates the EU-project "EXTRA: Exploiting eXascale Technology with Reconfigurable Architectures" within the European Horizon 2020 programme FETHPC (Future and Emerging Technologies Proactive programme Towards Exascale High Performance Computing). The project started September 1, 2015 and runs for three years, with a total budget of almost 4 million euro and a planned 567 person months of work.

Prof. Dirk Stroobandt is the project coordinator of the EXTRA project, involving also universities from the UK (Imperial College London and University of Cambridge), Greece (Telecommunications Systems Institute), Italy (Politecnico di Milano), the Netherlands (Universiteit van Amsterdam) and Germany (Ruhr-Universität Bochum), as well as companies from Greece (Synelixis) and the UK (Maxeler).

In the EXTRA project, we propose to create a new and flexible exploration platform for developing reconfigurable architectures and tools with run-time reconfiguration built-in from the start. The idea is to enable the joint optimization of architecture, tools, applications and reconfiguration technology in order to prepare for the necessary power-efficient HPC hardware nodes of the future. This includes:

- Using novel reconfiguration approaches for processing, BRAMs, special blocks and interconnection. These reconfiguration approaches allow speeding up the reconfiguration process and having targeted reconfiguration for specific reconfigurable functions.

## SINS: Sound Interfacing though the SWARM: first public workshop

**February 16, 2016**
**KU Leuven - ESAT, Belgium**

http://www.esat.kuleuven.be/sins/

The KU Leuven research groups MICAS, TELEMIC, AdvISe & DraMCo and the iMinds-VUB group ETRO kindly invite you for the first SINS public workshop.

**About the project:**
SINS is a strategic basic research project, supported by the IWT, aiming at the development of high-performance wireless distributed sensing solutions with a multi-year autonomous life-time, with a focus on distributed acoustic monitoring.

Within SINS, the conflicting requirements of high performance and long lifetime are pursued by relying on a swarm of collaborating low performance sensing nodes, which can quickly scale their performance according to the environmental conditions. This allows to achieve high-accuracy monitoring when required, while having very low average power consumption. The SINS concepts are demonstrated on acoustic activity monitoring and acoustic (location) tracking, and this in two use cases: 1.) AAL for Alzheimer monitoring, and 2.) acoustic surveillance and home automation.
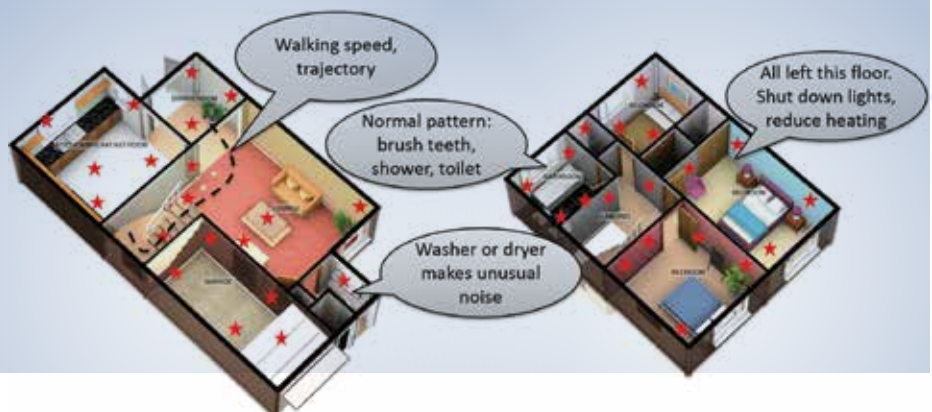
**About the workshop:**
The workshop will host presentations and demonstrations by the different research groups participating in the project on the achieved innovations up to now, including: the hardware and chip implementation of the (very low power) acoustic sensing node, the wireless subsystem, the embedded acoustic localization system, the efficient embedded sound classification with scalable computational workload and the acoustic sound source separation.

The realized innovations of the different partners are integrated into a joint acoustic localization and classification demonstrator with multiple collaborating acoustic sensor nodes. This will allow the attendees to experience the impact of the different findings in a full system set-up.

The workshop closes with presentations by some members from the 'Industrial Advisory Committee' which will testify on the potential of SINS technology in application domains such as Home Automation and e-Health.



Walking speed, trajectory

Normal pattern: brush teeth, shower, toilet

Washer or dryer makes unusual noise

All left this floor. Shut down lights, reduce heating

- A reconfigurable coarse grain architecture with as basic components processing, memory, and interconnection units of different complexity. The basic components can be those provided by current FPGAs but the system will also incorporate more complex components like basic CPUs, switches, caches that will also be instantiated and/or reconfigured on demand; those can be built-in or implemented on reconfigurable fabric.

- Just-in-time synthesis methods for reconfiguration on the fly. The whole system can be synthesized/reconfigured based on immediate application requirements. This requires a complete tool flow that targets this just-in-time synthesis. We aim at reducing the reconfiguration time so as to make reconfiguration more useful.

- Optimizations of applications with reconfiguration as an explicit design concept.

- The complete chain from device up to the application.

As part of our project, we offer the European research community a research platform with open source architecture descriptions and tools for continued research on reconfiguration and for finding the next-generation system requirements (a virtual tool environment – such as VPR). We want to provide the European platform for run-time reconfiguration to maintain Europe's competitive edge and leadership in run-time reconfiguration and reconfigurable computing.

The project also has an Industry Advisory Board (mainly looking at industrial applications of the reconfiguration concept) and a Research Advisory Board (mainly following up the platform research). People interested in being part of either Board can contact Prof. Dirk Stroobandt.

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