

taste

A real-time software engineering tool-chain
Overview, status and future

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what is taste?



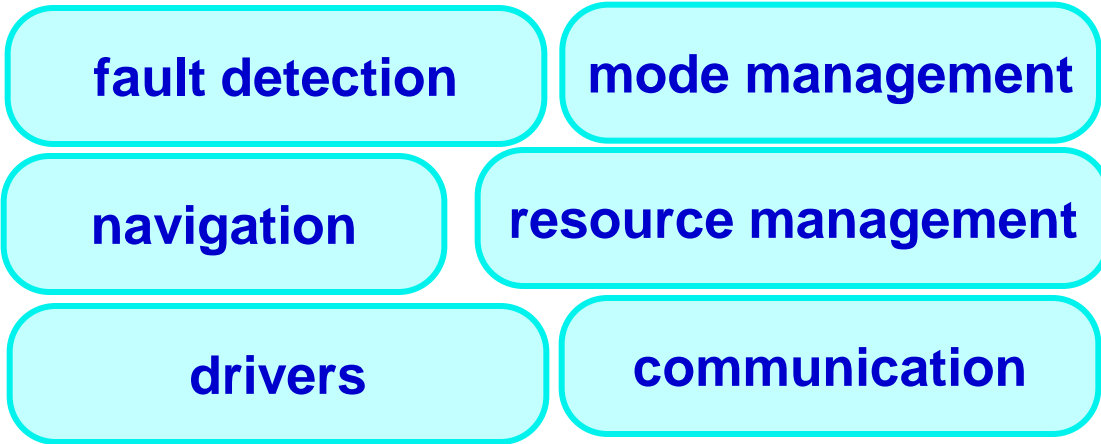
- A software engineering tool-chain targeting heterogeneous systems
- A set of tools to build and validate embedded, real-time systems
- A concentrated set of technology, available for free and open source

taste

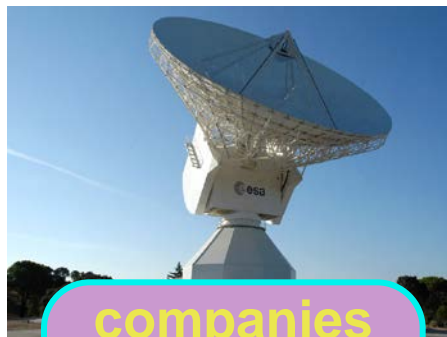
The Assert Set of Tools for Engineering



heterogeneous systems (1)



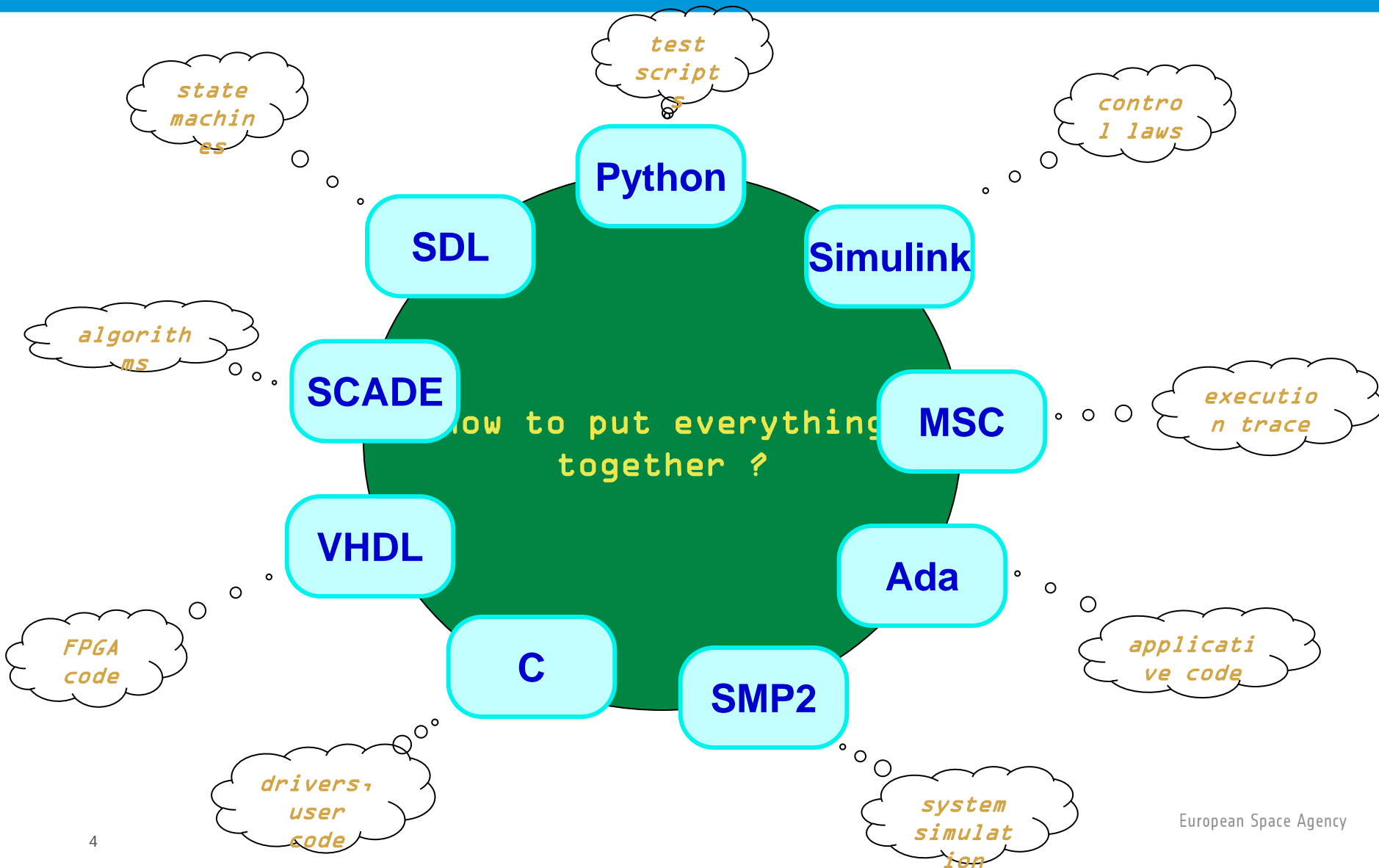
companies
X, Y, Z...



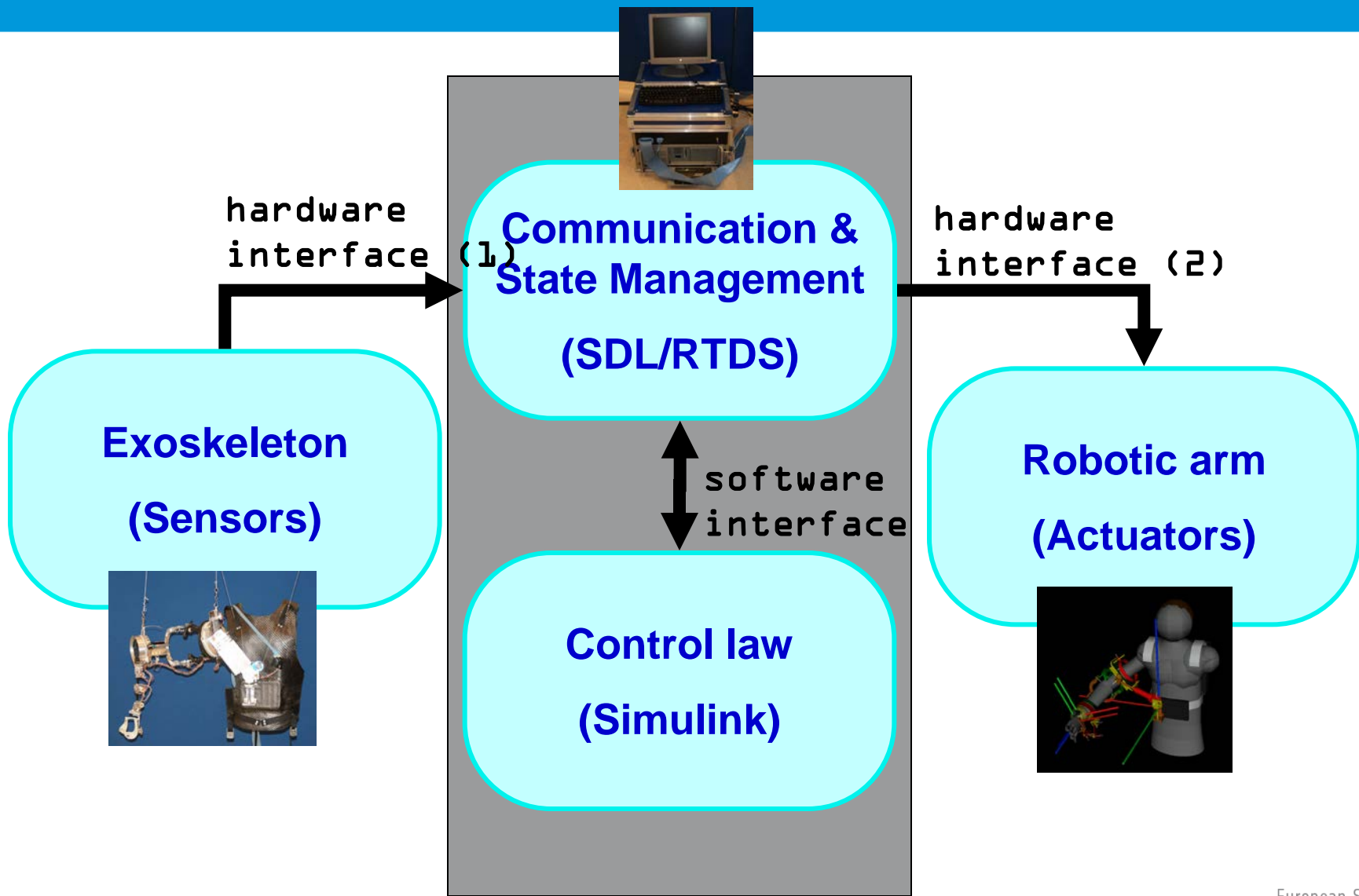
companies
A, B, C

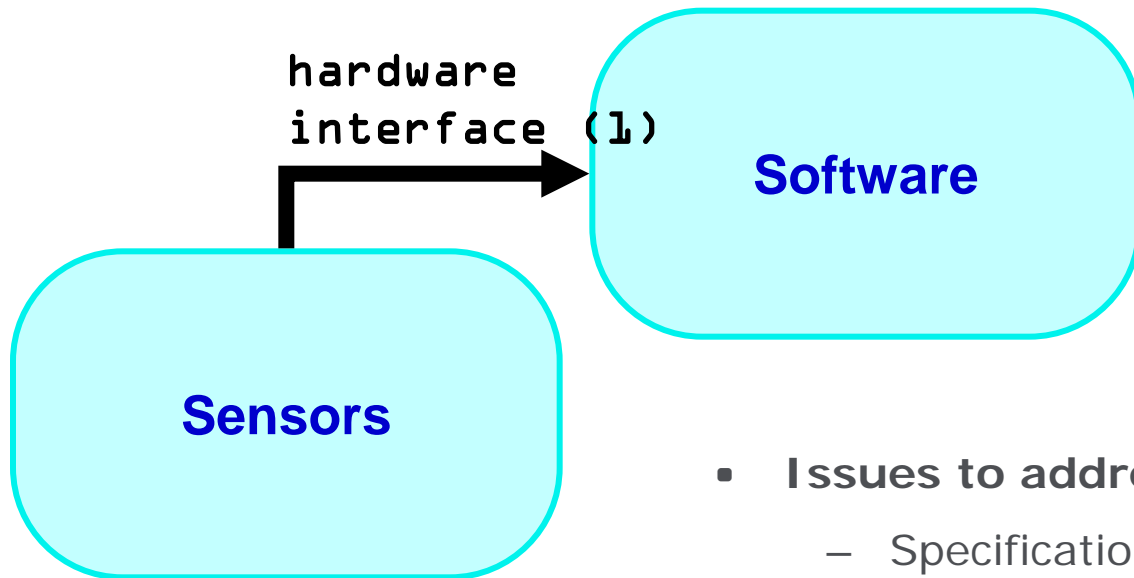


heterogeneous systems needs (2)

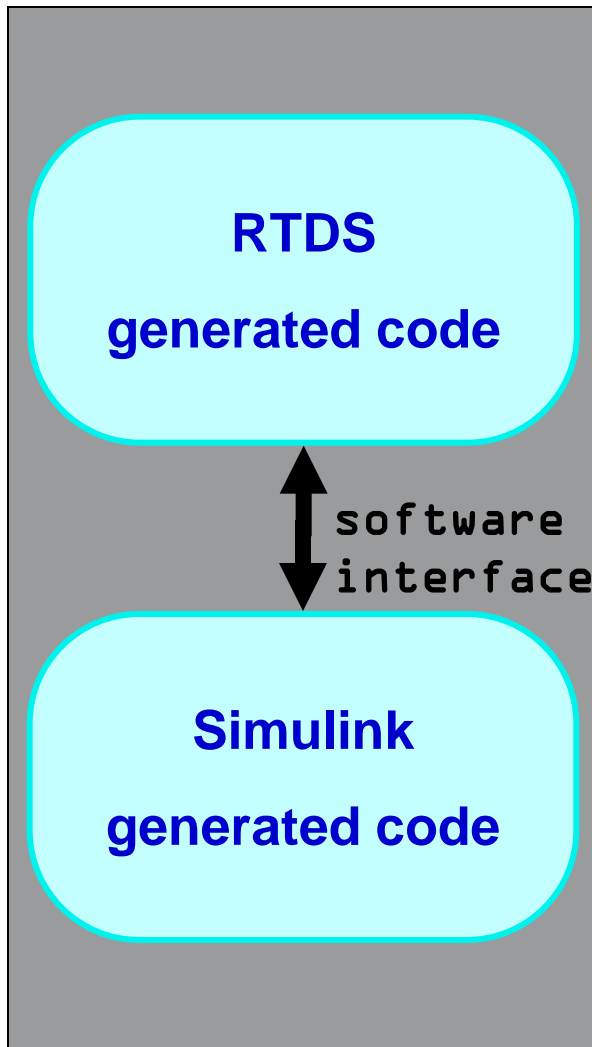


- **Manually?**
 - Requires a lot of hacking
 - Difficult maintenance in case of interface changes
 - That is the most common way of doing
- **Using a commercial modelling tool?**
 - No support for heterogeneous models (at best, Simulink integration)
 - No support for sensor/actuators interfacing
- **Using TASTE**





- **Issues to address:**
 - Specification of the interface (logical message description)
 - Message physical representation (binary stream)
 - imposed by the hardware.
 - Conversion to a software data structure



- **Issues to address:**

- 1) Specification of the interface (logical message description)
- 2) Conversion at model level (keep the same semantics in both RTDS and Simulink)
- 3) Conversion at code level: map each field of the interface from one generated piece of code to the other

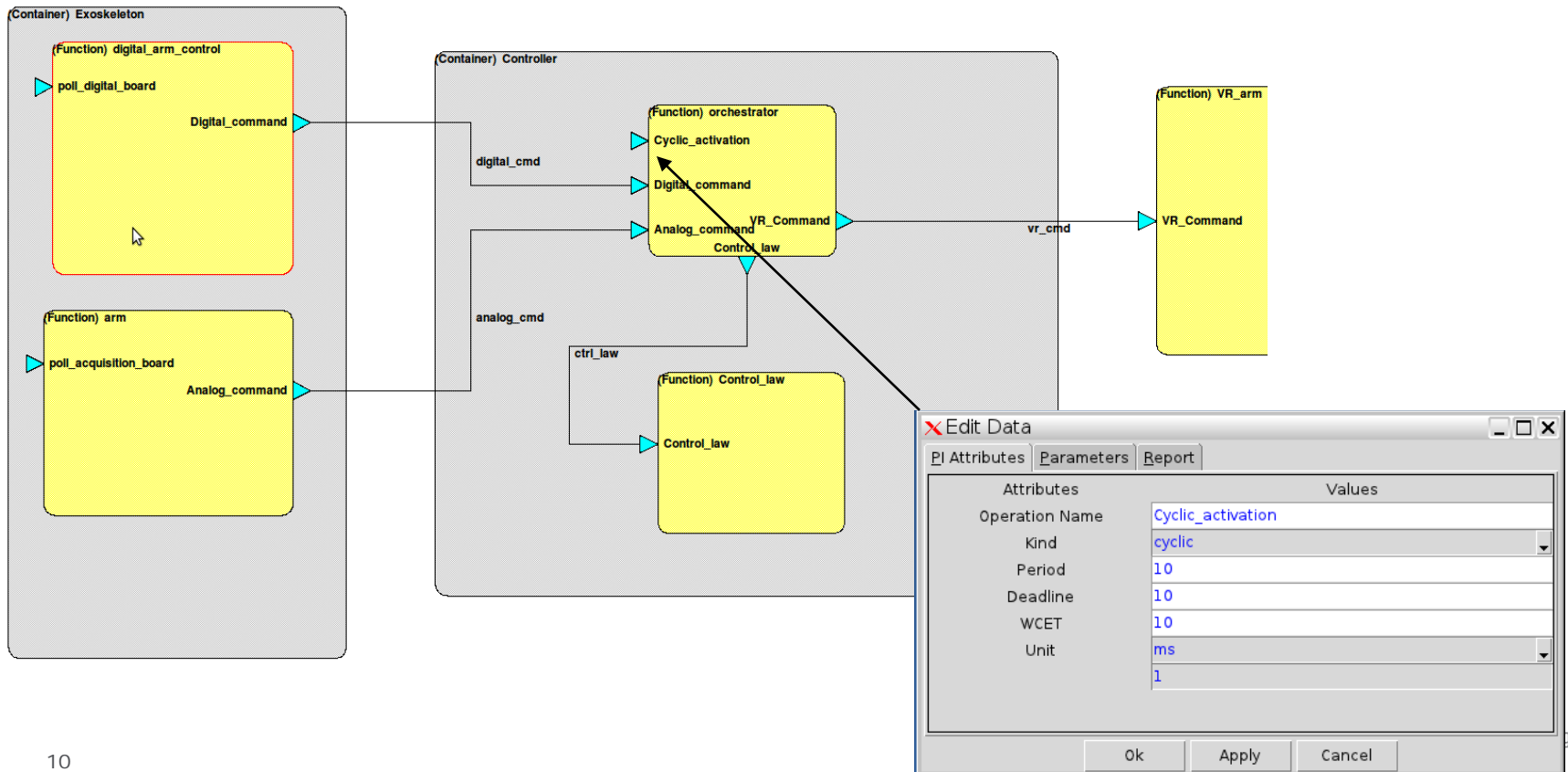
- TASTE solves integration issues by allowing all hardware and software pieces to communicate together transparently
- TASTE relies on two key formally-defined languages:

ASN.1

AADL

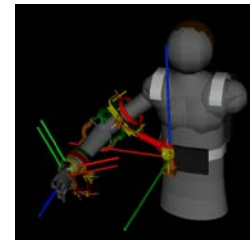
- TASTE relies on a clear and sound process
- TASTE is designed to be used by non-software specialists
- TASTE does not reinvent the wheel: it uses existing, proven technologies (SDL, MSC, SCADE...) and put them together in order to build and validate homogeneous systems

- A textual notation to capture all the attributes of a system
- TASTE provides a graphical view of AADL files



ASN.1 to describe interfaces

- A simple notation to describe software and hardware interfaces
- Our tools generate code for embedded systems (no malloc, no system call, support for C and [Spark] Ada)



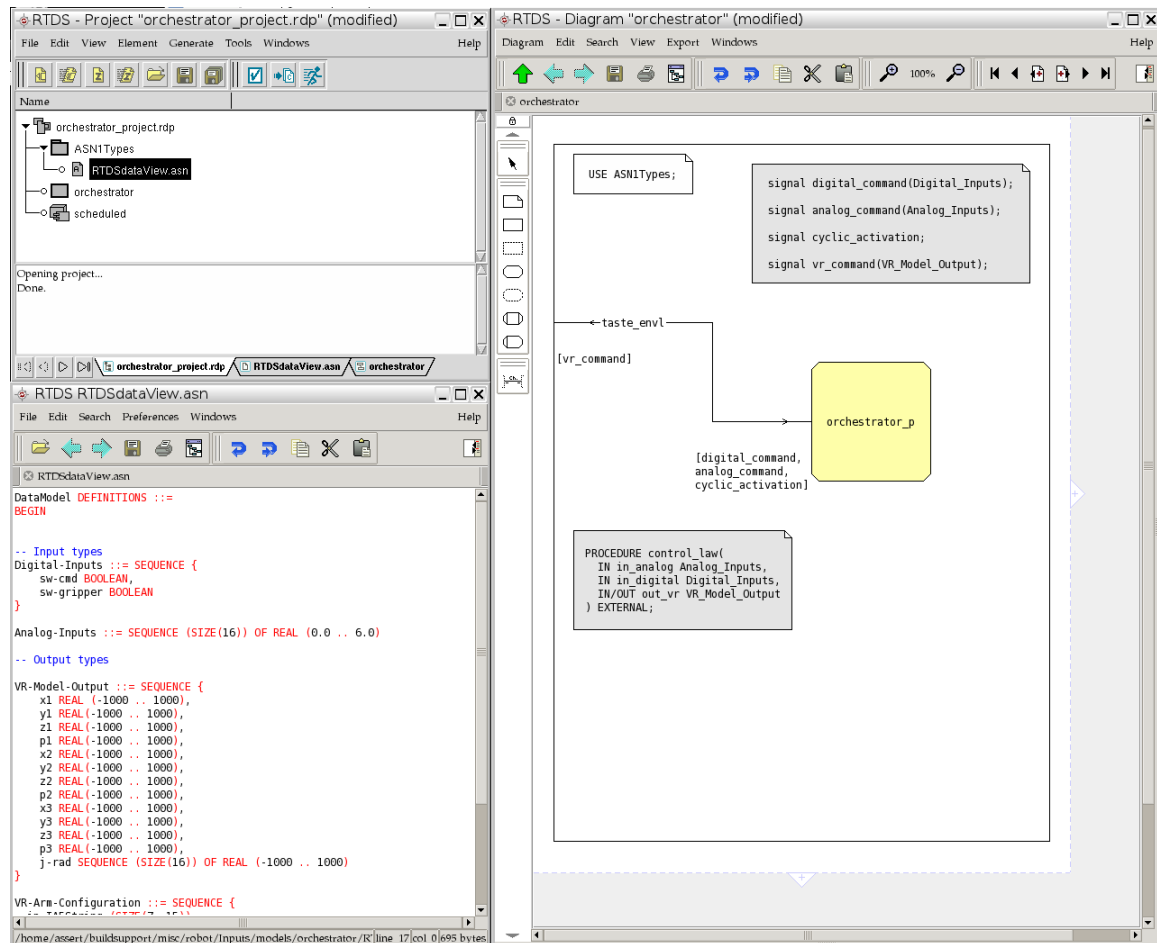
```
dataview.asn
13 -- Output types
14
15 VR-Model-Output ::= SEQUENCE {
16   x1 REAL (-1000 .. 1000),
17   y1 REAL (-1000 .. 1000),
18   z1 REAL (-1000 .. 1000),
19   p1 REAL (-1000 .. 1000),
20   x2 REAL (-1000 .. 1000),
21   y2 REAL (-1000 .. 1000),
22   z2 REAL (-1000 .. 1000),
23   p2 REAL (-1000 .. 1000),
24   x3 REAL (-1000 .. 1000),
25   y3 REAL (-1000 .. 1000),
26   z3 REAL (-1000 .. 1000),
27   p3 REAL (-1000 .. 1000),
28   j-rad SEQUENCE (SIZE(16)) OF REAL (-1000 .. 1000)
29 }
--
```



```
dataview-uniq.acn
/*Output types*/
VR-Model-Output [{
  j-rad [size 16] {
    dummy [encoding IEEE754-1985-64, endianness little]
  },
  p1 [encoding IEEE754-1985-64, endianness little] ,
  p2 [encoding IEEE754-1985-64, endianness little] ,
  p3 [encoding IEEE754-1985-64, endianness little] ,
  x1 [encoding IEEE754-1985-64, endianness little] ,
  x2 [encoding IEEE754-1985-64, endianness little] ,
  x3 [encoding IEEE754-1985-64, endianness little] ,
  y1 [encoding IEEE754-1985-64, endianness little] ,
  y2 [encoding IEEE754-1985-64, endianness little] ,
  y3 [encoding IEEE754-1985-64, endianness little] ,
  z1 [encoding IEEE754-1985-64, endianness little] ,
  z2 [encoding IEEE754-1985-64, endianness little] ,
  z3 [encoding IEEE754-1985-64, endianness little]
}
}
```

start the real work from function skeletons

- Supported languages: SDL (RTDS, ObjectGEODE), SCADE, Simulink, C, Ada, VHDL



The screenshot displays the RTDS software interface. The left pane shows a project tree with files like 'orchestrator_project.rdp', 'ASNI Types', 'RTDSdataView.asn', 'orchestrator', and 'scheduled'. The bottom pane shows the source code for 'RTDSdataView.asn', which includes data model definitions for digital and analog inputs, VR model outputs, and VR arm configurations.

```
DataModel DEFINITIONS ::=
BEGIN

-- Input types
Digital-Inputs ::= SEQUENCE {
  sw-cmd BOOLEAN,
  sw-gripper BOOLEAN
}

Analog-Inputs ::= SEQUENCE (SIZE(16)) OF REAL (0.0 .. 6.0)

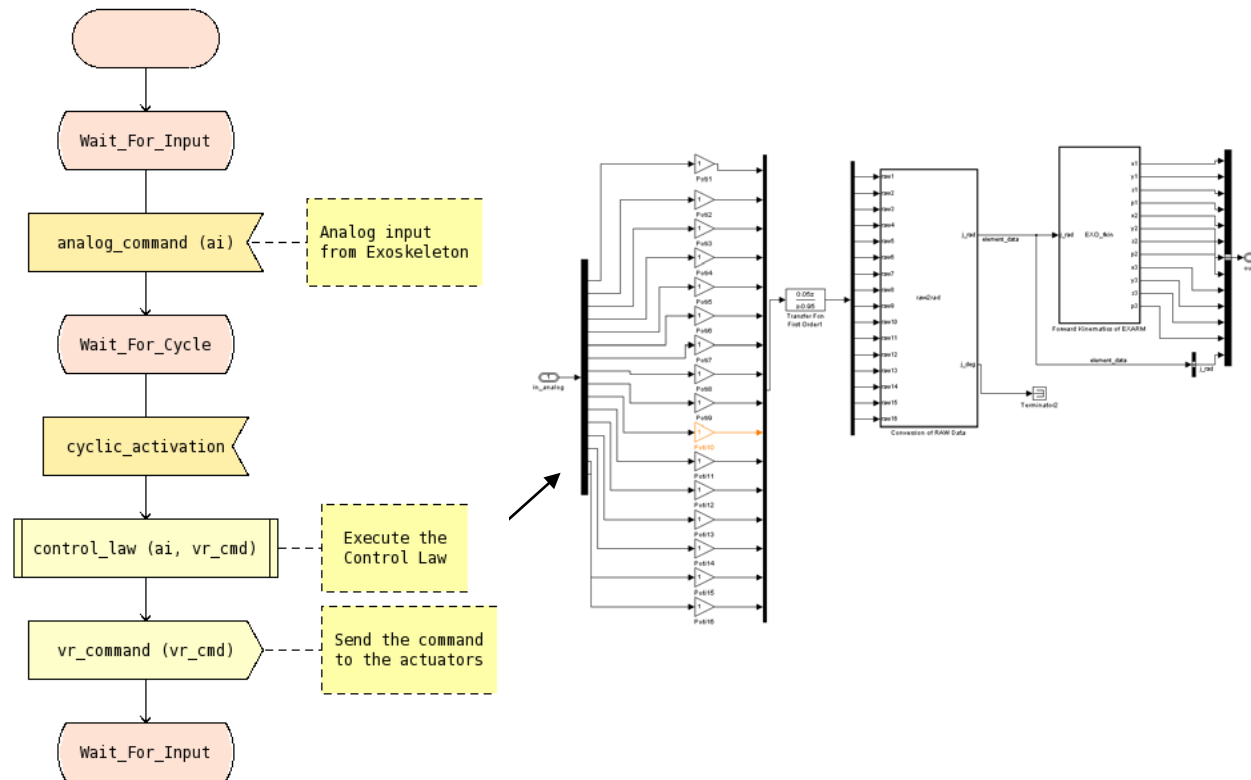
-- Output types
VR-Model-Output ::= SEQUENCE {
  x1 REAL (-1000 .. 1000),
  y1 REAL (-1000 .. 1000),
  z1 REAL (-1000 .. 1000),
  p1 REAL (-1000 .. 1000),
  x2 REAL (-1000 .. 1000),
  y2 REAL (-1000 .. 1000),
  z2 REAL (-1000 .. 1000),
  p2 REAL (-1000 .. 1000),
  x3 REAL (-1000 .. 1000),
  y3 REAL (-1000 .. 1000),
  z3 REAL (-1000 .. 1000),
  p3 REAL (-1000 .. 1000),
  j-rad SEQUENCE (SIZE(16)) OF REAL (-1000 .. 1000)
}

VR-Arm-Configuration ::= SEQUENCE {
  -- ...
}
```

The right pane shows a diagram titled 'orchestrator'. It features a yellow block labeled 'orchestrator_p' with an arrow pointing to it from a box containing the text '[vr_command]'. Above the block, a box lists signals: 'signal digital_command(Digital_Inputs);', 'signal analog_command(Analog_Inputs);', 'signal cyclic_activation;', and 'signal vr_command(VR_Model_Output);'. Below the block, a box contains the procedure definition: 'PROCEDURE control_law(IN in_analog Analog_Inputs, IN in_digital Digital_Inputs, IN/OUT out_vr VR_Model_Output) EXTERNAL;'. A note at the top left of the diagram says 'USE ASNI Types;'. The diagram also shows a signal flow from 'taste_envl' to the 'orchestrator_p' block.

Mix languages to get the best of all worlds – no “unified language” to rule them all!

- The robotic case study mixes C (drivers), SDL (RTDS – system overall orchestration and logic) and Simulink (control laws)



A straightforward process



1) Describe interfaces with ASN.1

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- 2) **Capture the logical architecture using the AADL editor (*Interface View*)**

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- 3) Generate code skeletons and write the deployment code
- 4) **Capture the system hardware and deployment (*Deployment View*)**

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- 4) Capture the system hardware and deployment (*Deployment View*)
- 5) **Verify system feasibility using TASTE-provided tools (Cheddar, MAST, REAL)**

A straightforward process

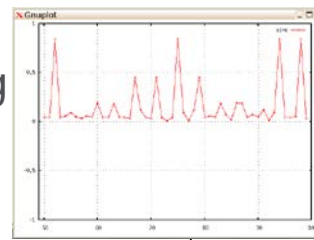


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- 6) Build the system and download it on target**

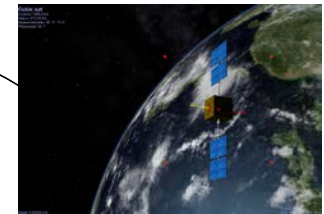
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- 7) Analyze system performance at run-time**

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- 7) Analyze system performance at run-time
- 8) Validate implementation regarding specifications**

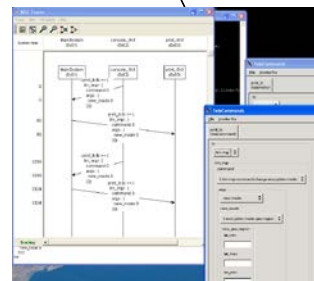
- Auto-GUI generation
- MSC tracing and recording
- Plot streaming
- Testing via python scripts
- Code coverage
- Profiling
- Task analysis
- 3D rendering



GNUPlot streaming



Celestia rendering



GUI and MSC control

```
from DataView_asn import *  
  
def testDeal(val):  
    # Create a stream buffer to host the encoded data  
    d1 = DataStream(DV.T_REAL_REQUIRED_BYTES_FOR_ENCODING)  
    # Create a T_REAL  
    f1 = T_REAL()  
    # Set the value  
    f1.Set(val)  
    try:  
        # Encode the value of f1 into the buffer d1  
        f1.Encode(d1)  
    except:  
        print "Encoding failed..."  
        sys.exit(1)  
  
    binaryData = d1.GetPyString() # Get the encoded stream bytes  
    # as a Python string. You can  
    # pass these data over sockets,  
    # save them to files, etc
```

Python test scripts

- In addition to ESA, TASTE main contributors are
 - Semantix (GR)
 - Ellidiss (F)
 - ISAE (F), ENST (F)
 - UPM (ES)
- TASTE is available freely and open source
 - Ensure long-term support
- It can be downloaded from:
 - **www.assert-project.net/taste**



For more information:
www.assert-project.net/taste